DETERMINISTIC TESTING OF EDGE-TRIGGERED LOGIC

ABSTRACT OF THE DISCLOSURE

A digital system having multiple clock domain, each including at least one edge-triggered device, such as a flip-flop, is structured to be submitted to scan testing. Each data path from one clock domain to another includes a latch that is operated by a test clock. During scan testing, when the digital system is logically reconfigured to form one or more scan chains for receiving a test vector, the latches are operated to ensure that the test vector is passed from one domain to another.

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